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MS-7704

Mini-ITX Ver: 2.4

CPU:

INTEL-Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point H61

OnBoard Chipset:

HD Audio Codec:ALC892

uPD720202 USB3.0

LAN-RTL8111E

SIO:Fintek F71889AD

Flash ROM: 64 Mb SPI

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

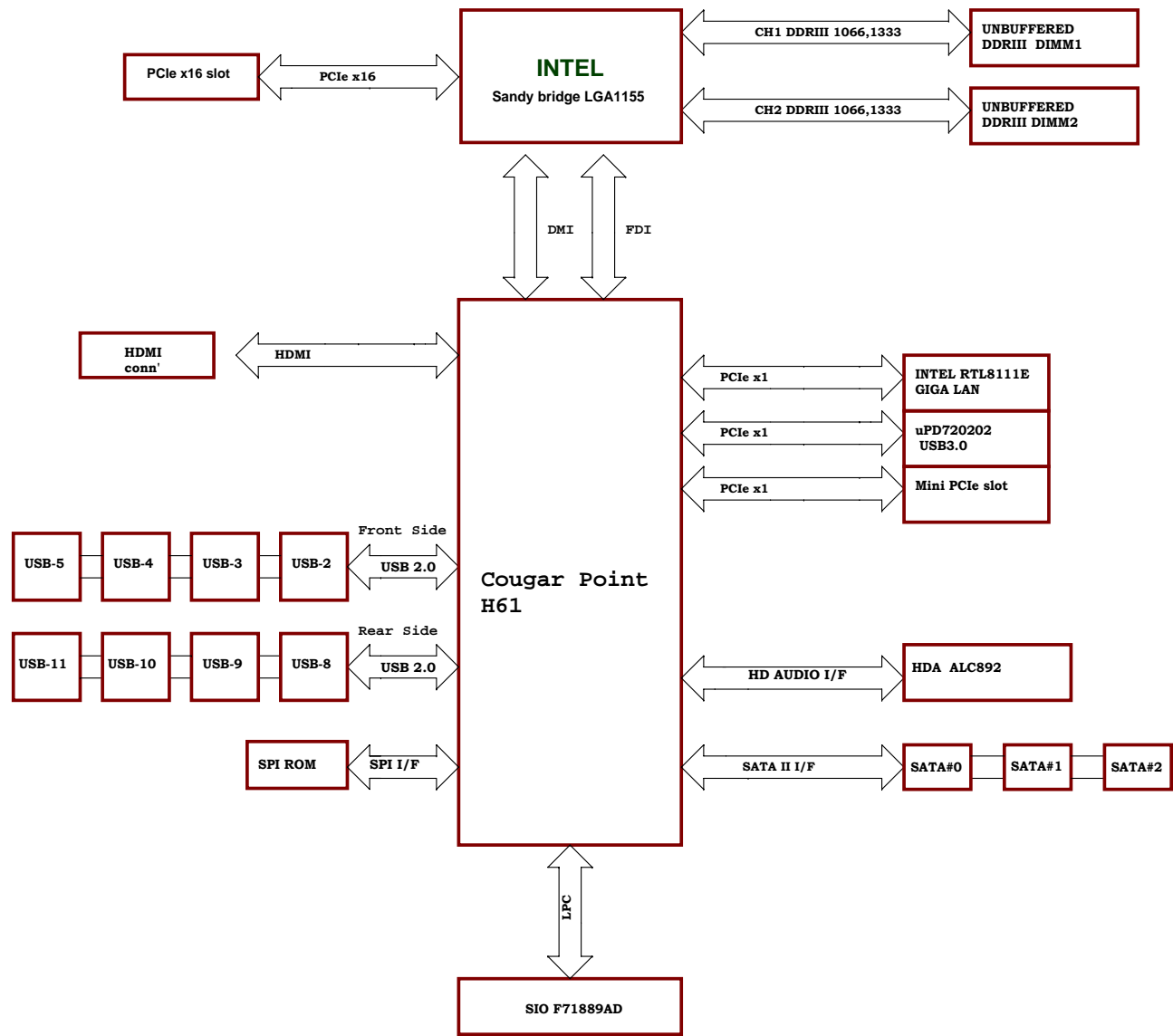
Expansion Slots:

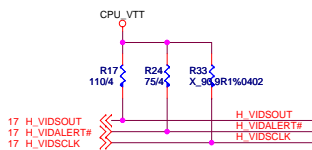
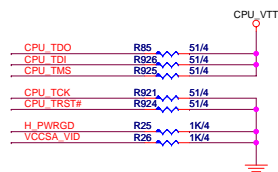
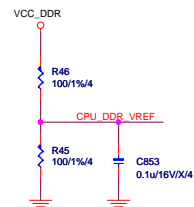
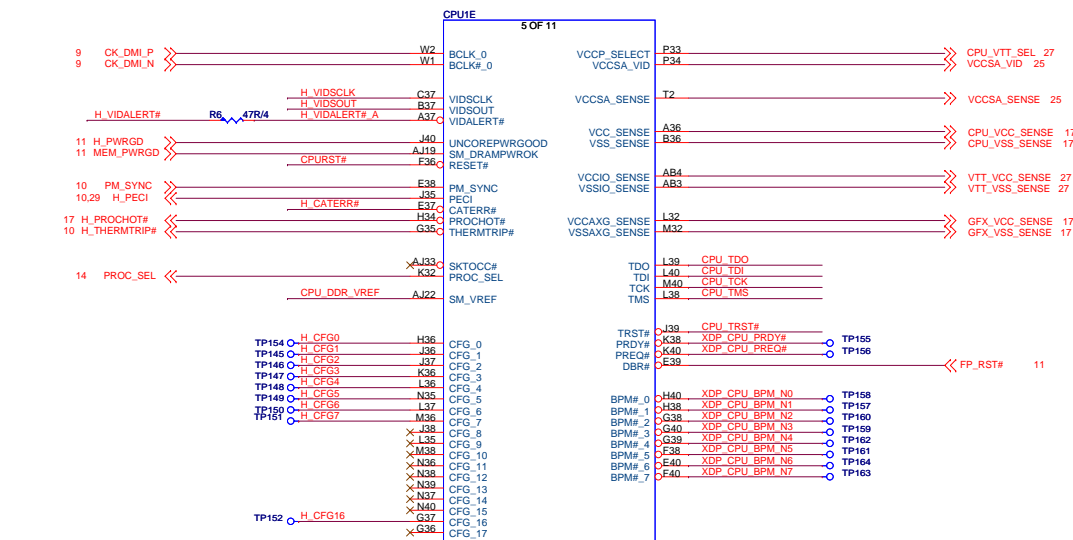
PCI Express (X16) Slot * 1

Mini PCIe(X1) Slot * 1

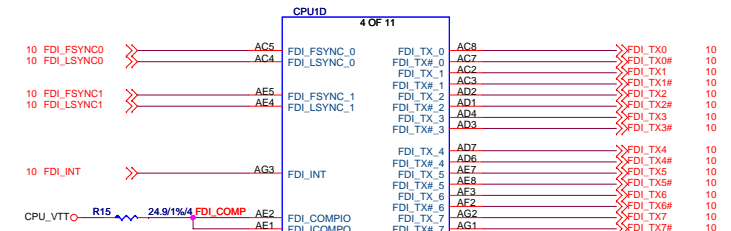
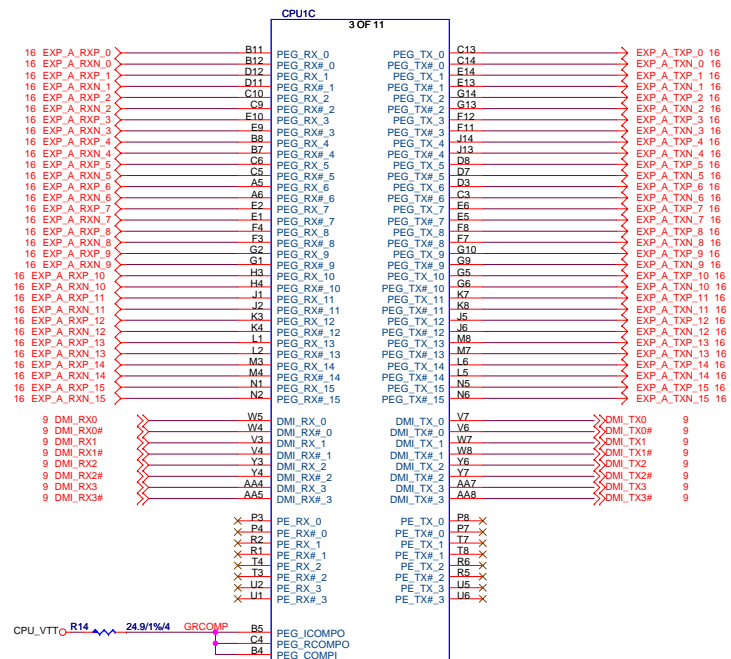
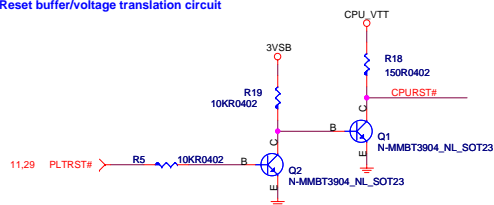
PWM:

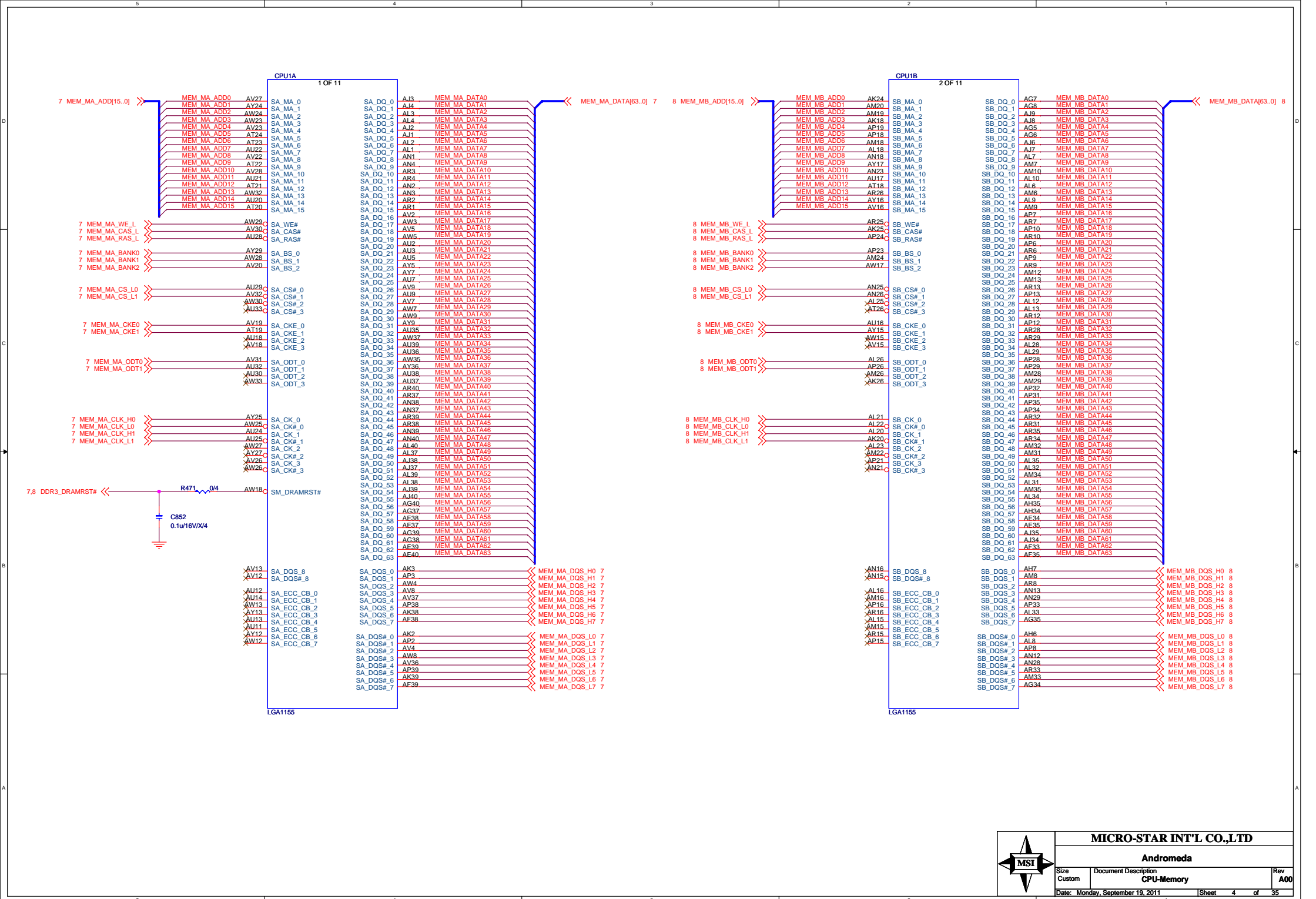
VRD12 ISL6364 4+1 Phase Dr.MOS

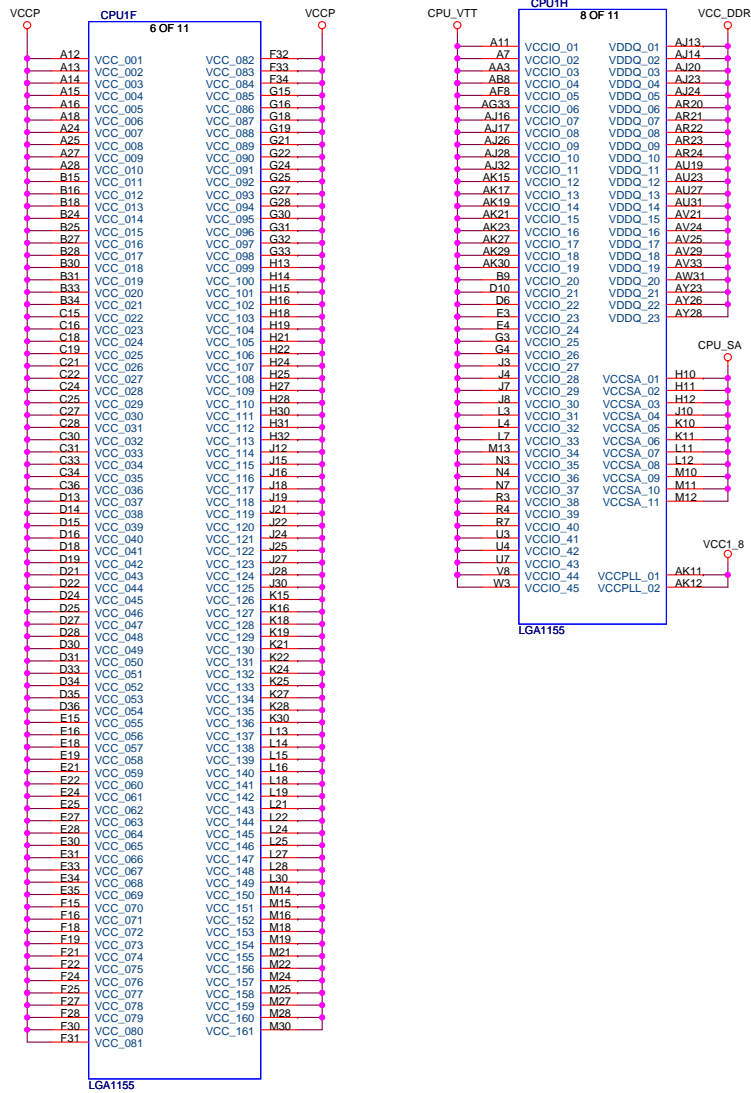




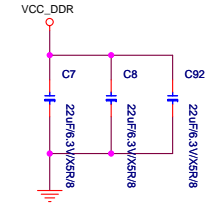
Reset buffer/voltage translation circuit





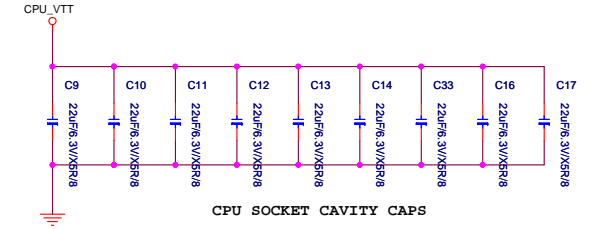


+1.5V_DDR3-Decoupling

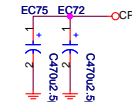


CPU SOCKET CAVITY CAPS

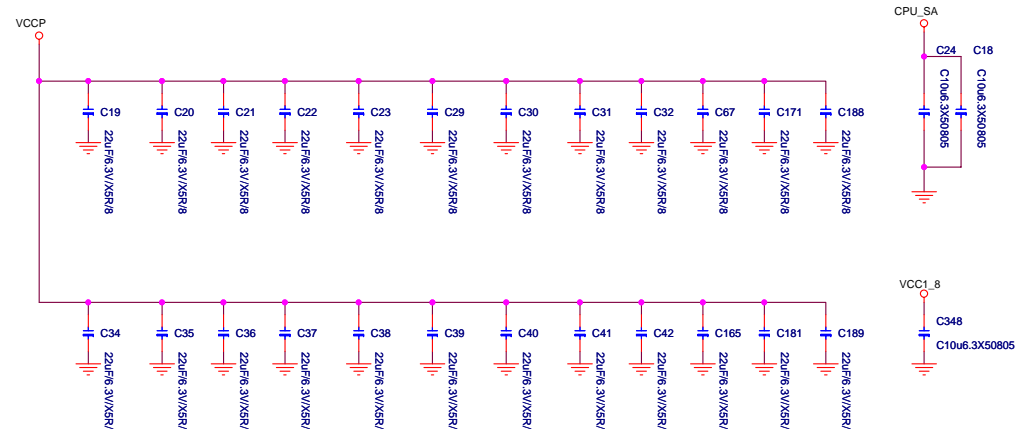
+CPU_VTT Decoupling



bottom SP Capacitors



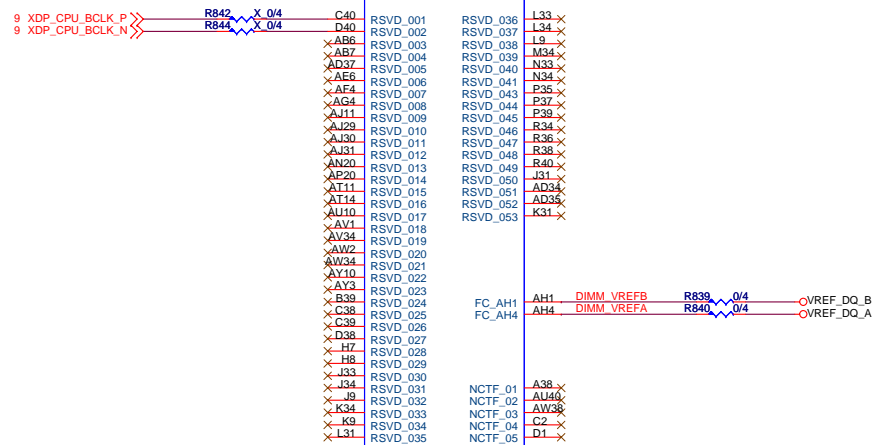
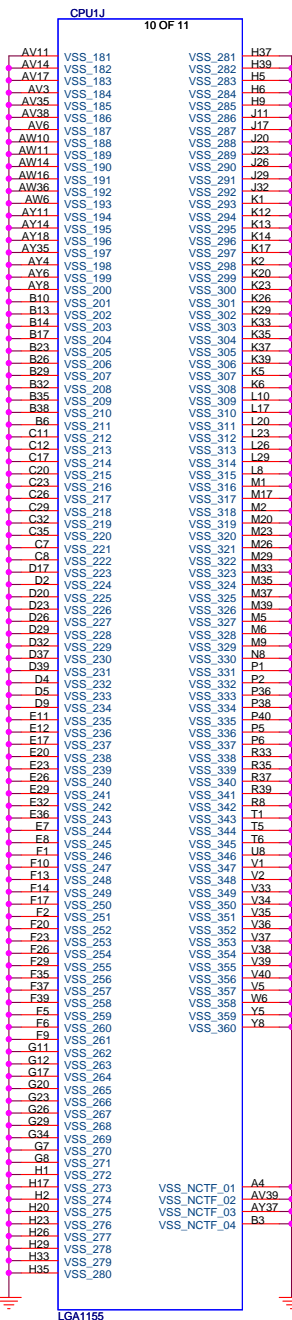
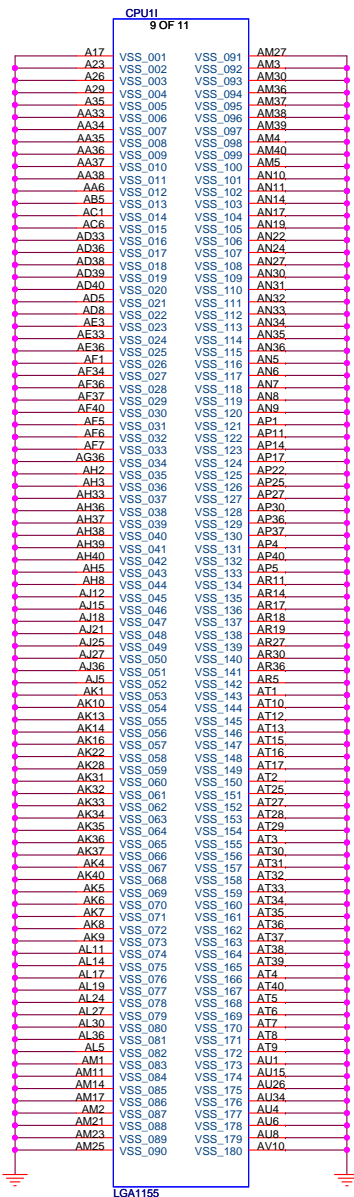
+CPU_VCCP-Decoupling

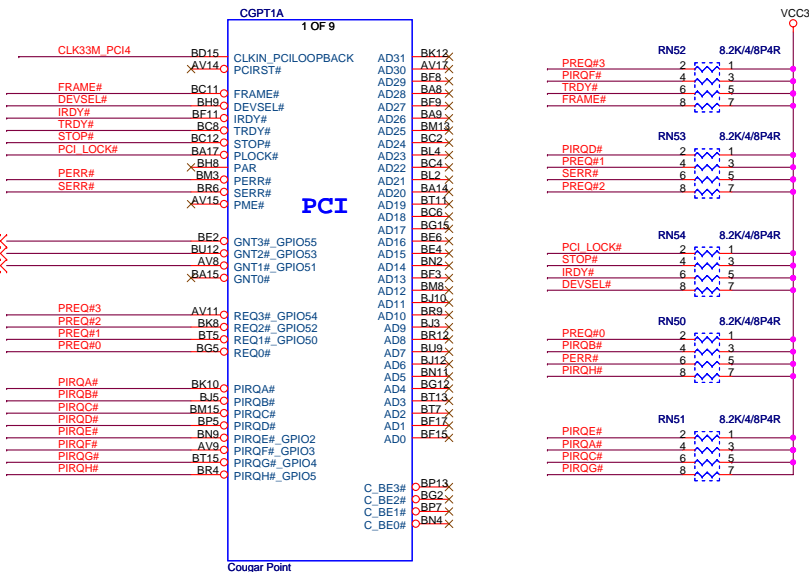
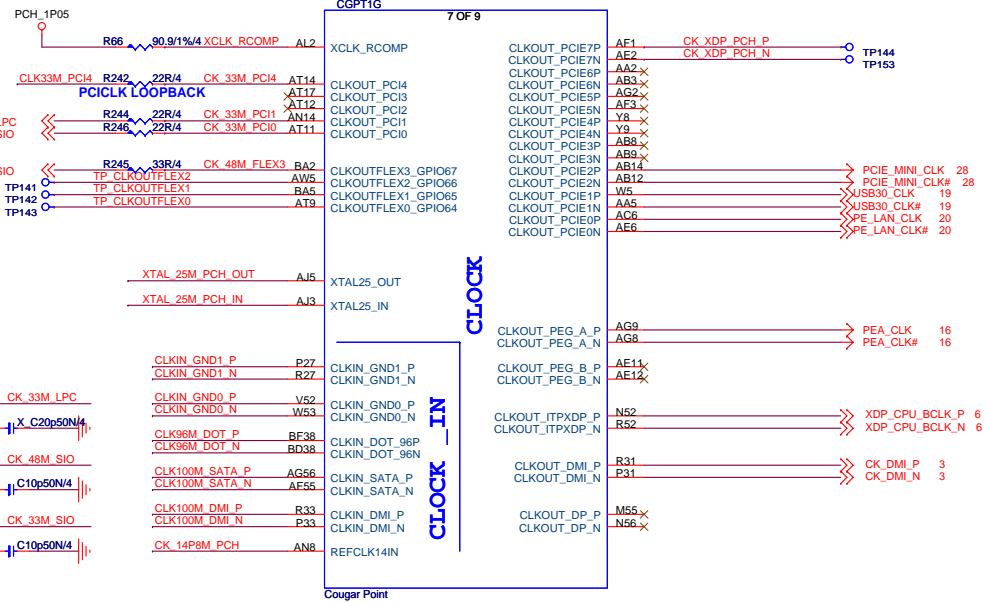
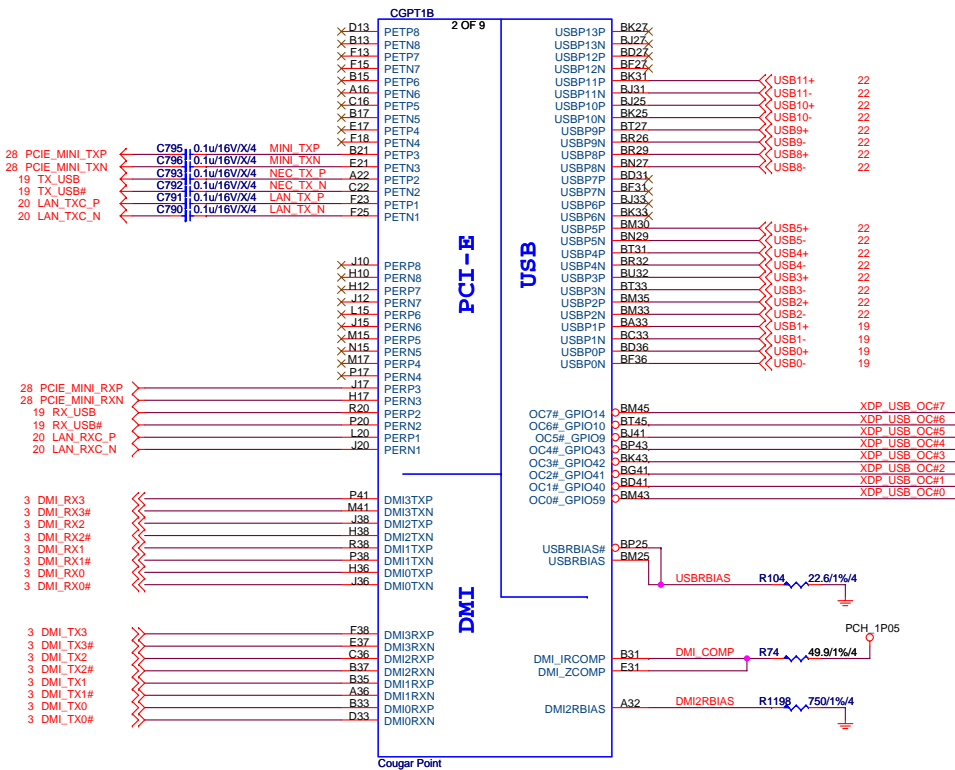


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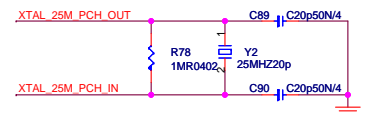
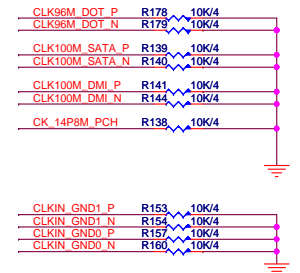
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Custom	CPU-Power	A00
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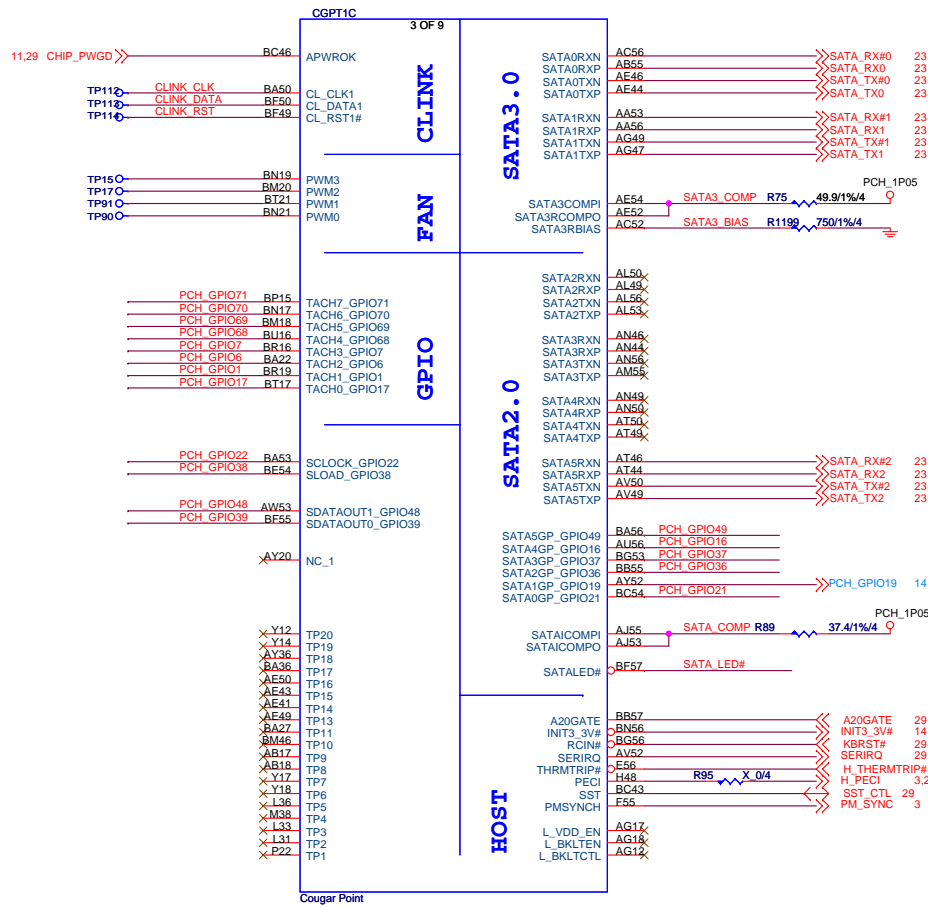
No Clock In Pull Down



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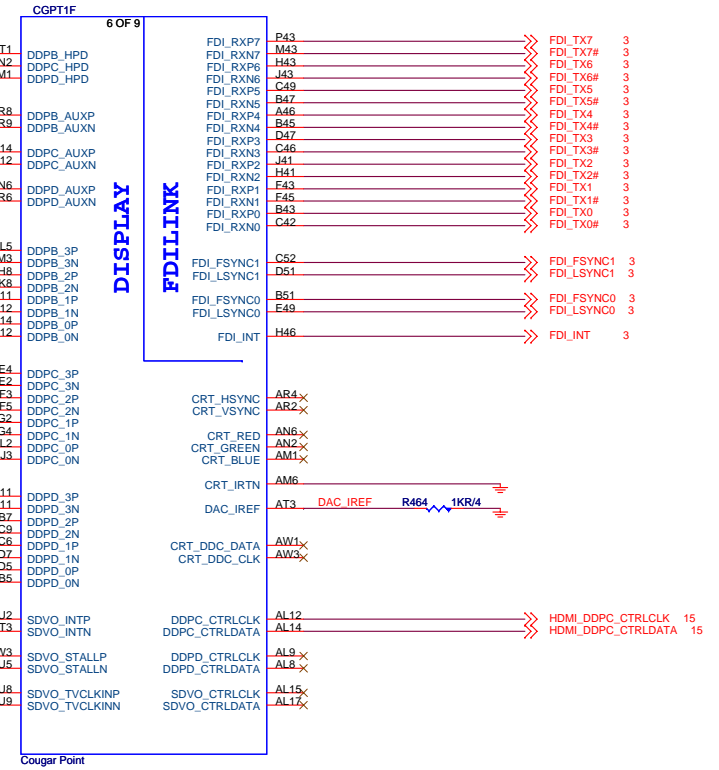
Andromeda

Size	Document Description	Rev
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Date:	Monday, September 19, 2011	Sheet 9 of 35

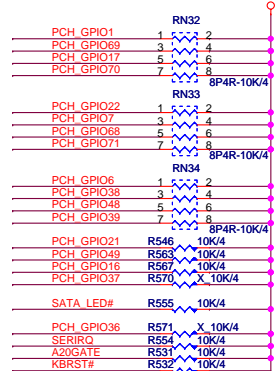


15 HDMI_DDPD_HPD >>

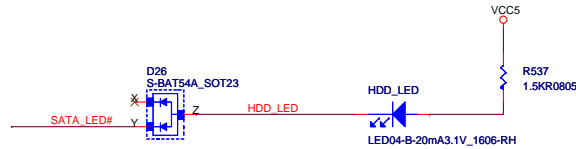
15 HDMI_DDPD_CLK_P
15 HDMI_DDPD_CLK_N
15 HDMI_DDPD_TX2_P
15 HDMI_DDPD_TX2_N
15 HDMI_DDPD_TX1_P
15 HDMI_DDPD_TX1_N
15 HDMI_DDPD_TX0_P
15 HDMI_DDPD_TX0_N



Pull HIGH for PCH



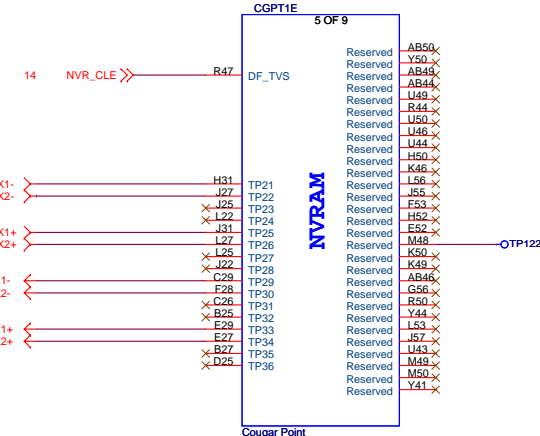
HDD LED



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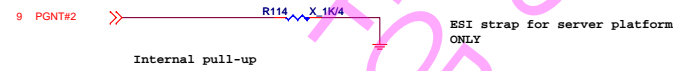
Size	Document Description	Rev
Custom	PCH-SATA/HOST/FAN/GPIO	A00
Date: Monday, September 19, 2011	Sheet 10 of 35	



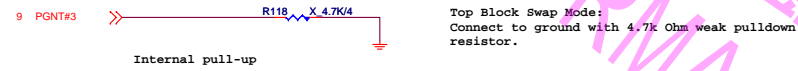
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	0
SPI	1	1



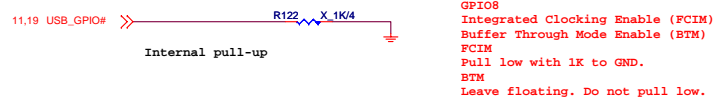
WEAK INTERNAL PULLUPS ON GNT1#



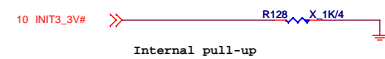
Internal pull-up



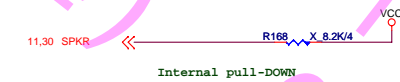
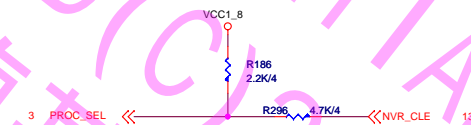
Internal pull-up



Internal pull-up



Internal pull-up



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0: Disable Internal Deep Sleep 1.05 V regulators.
1: Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

HDA_SYNC
On die PLL VR voltage selector

GPIO15
Default (Disable TLS):
Leave NC. Internal pull down.

DMI/FDI TERMINATION VOLTAGE
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH

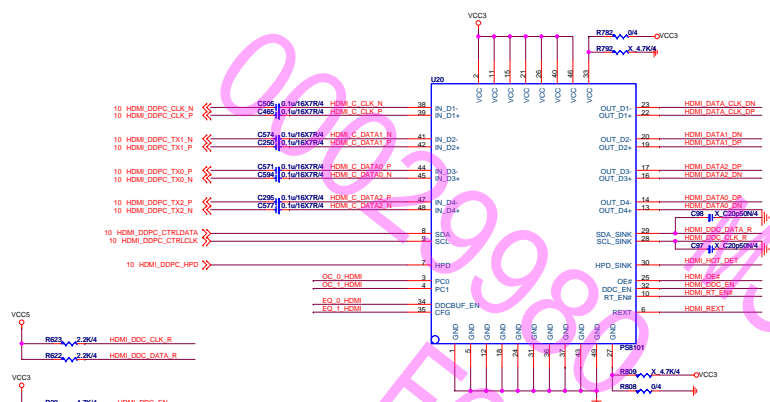
No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



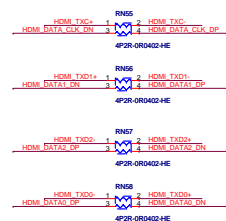
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Custom	PCH-STRAPS	A00
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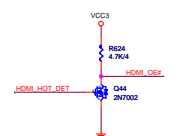
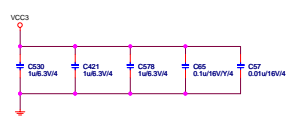
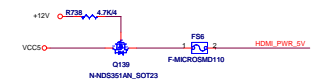
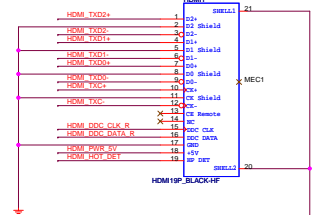
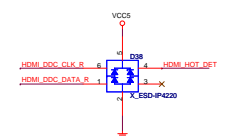


PARADE PN:B0B-081010C-P97

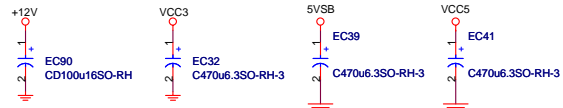
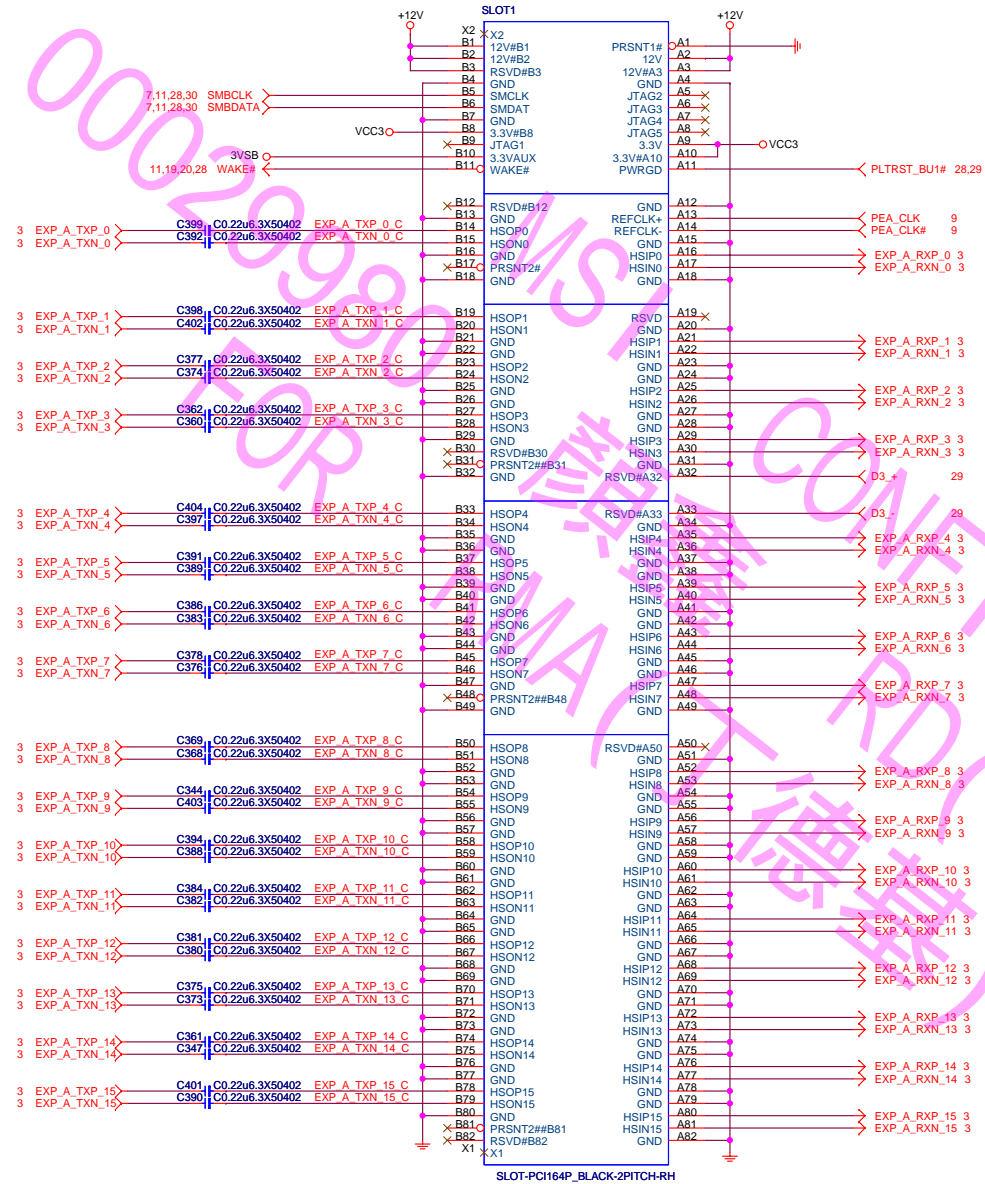



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	input 50 ohm termination resistor enable	the input termination resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCREF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

DDC_EN, DDCREF_EN, OE#	DDC Passive Switch	DDC Active Buffer	PCI, PC0	note
1, 0, X	On	Off	00	8 dB
1, 1, 0	Off	On	01	4 dB
1, 1, 1	Off	Off	10	12 dB
0, X, X	Off	Off	11	0 dB

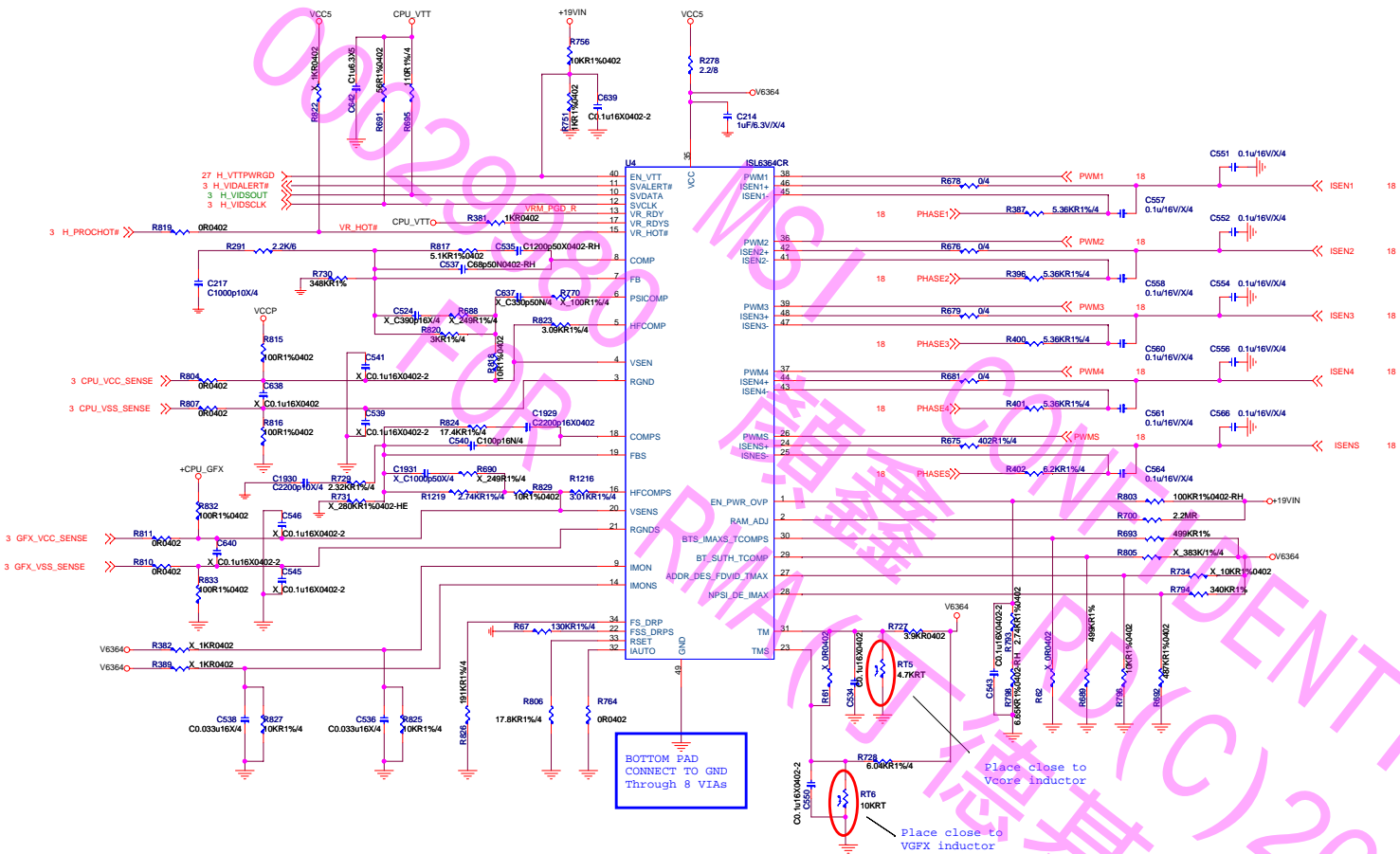


PCI EXPRESS X16 SLOT

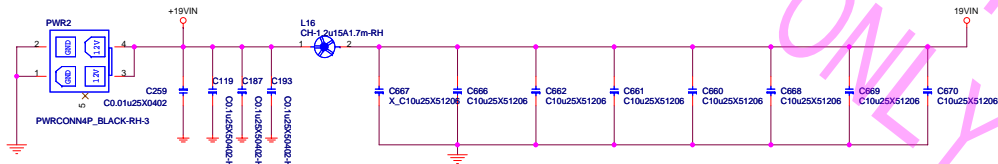
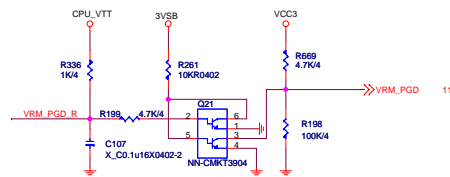


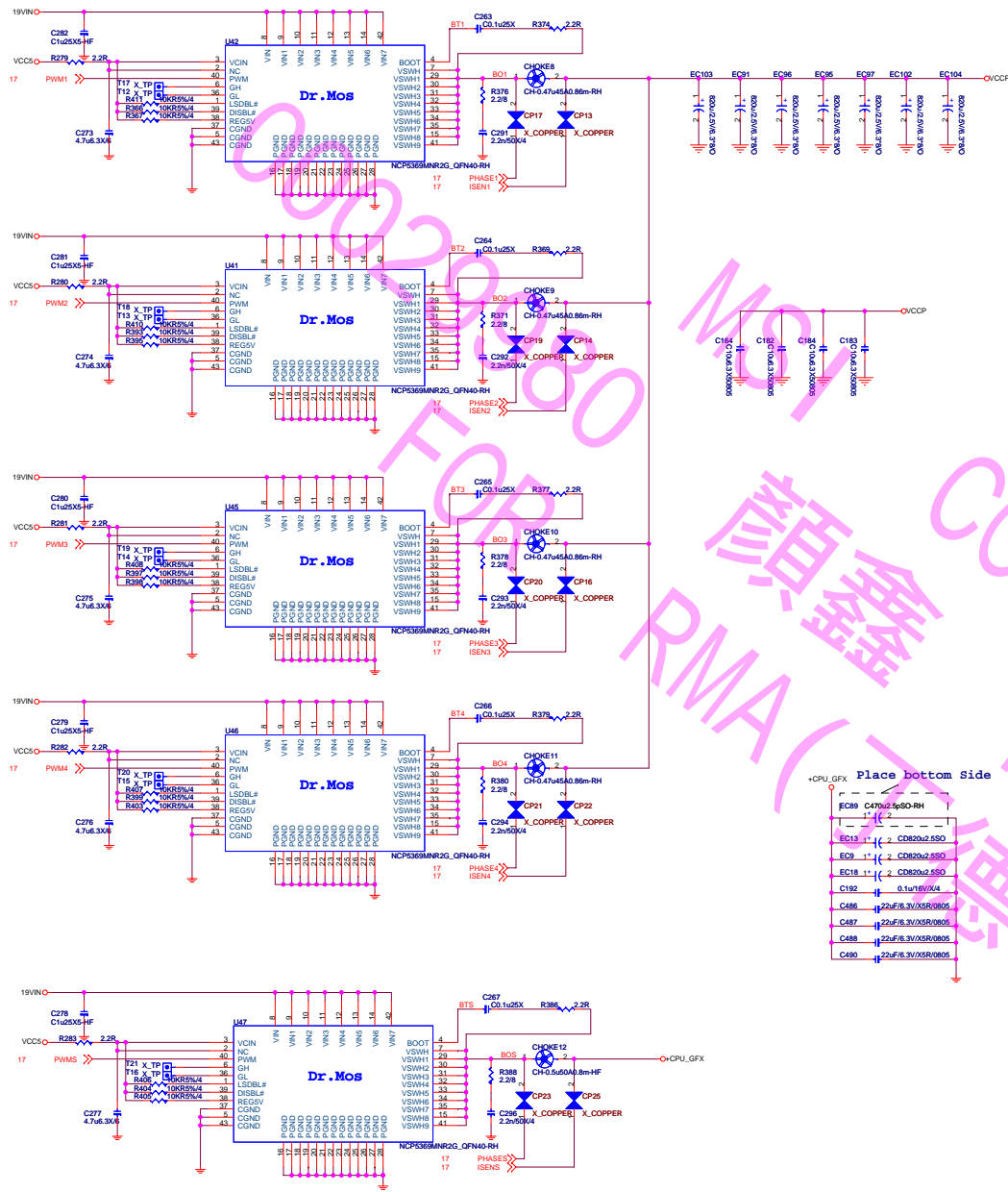
			MICRO-STAR INT'L CO.,LTD	
Andromeda				
Size	Document Description			Rev
Custom	PCIEx16 slot			A00
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VOLTAGE REGULATOR MODULE (VRD12)



VRMPWRGD LEVEL SHIFT





+CPU_GFX Place bottom Side

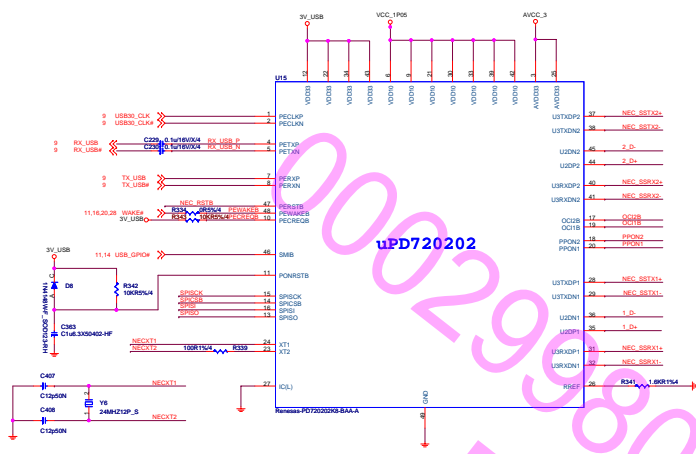
EC89	C470u2.5pSO-RH	1* (2
EC13	1* (2	CD820u2.5SO
EC9	1* (2	CD820u2.5SO
EC18	1* (2	CD820u2.5SO
C192	0.1u/16V/X4	
C486	22uF/6.3V/X5R/0805	
C487	22uF/6.3V/X5R/0805	
C488	22uF/6.3V/X5R/0805	
C490	22uF/6.3V/X5R/0805	



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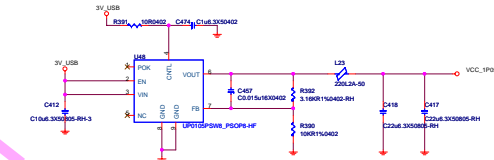
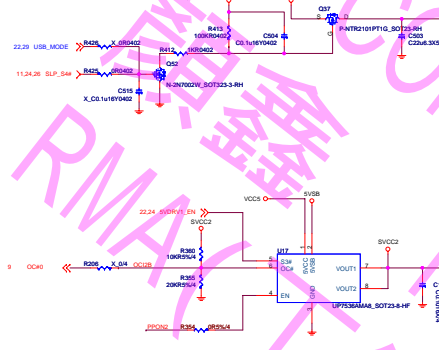
Andromeda

Site	Document Description	Rev
Custom	Dr.MOS	A00
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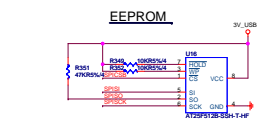
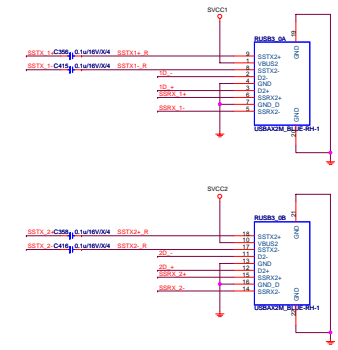


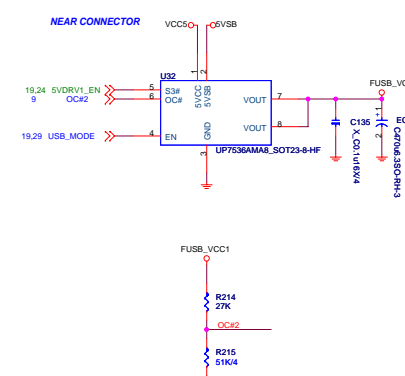
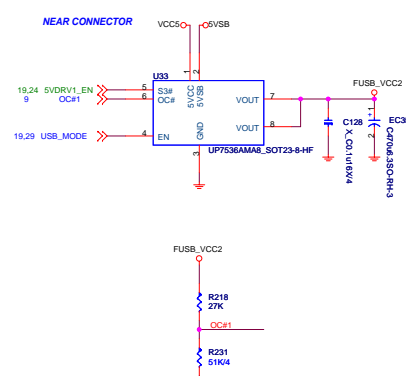
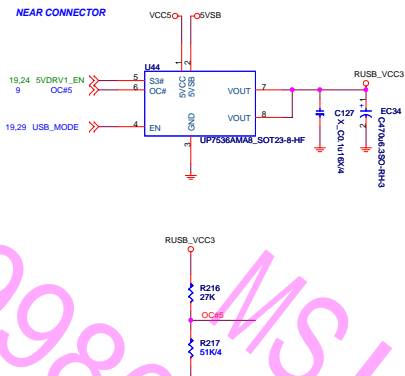
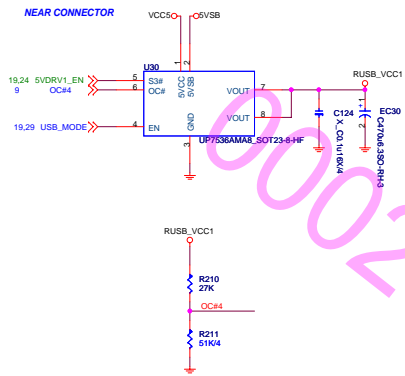
uPD720202

3V Dual Circuit

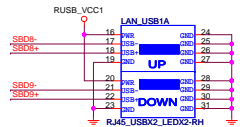


REAR USB3.0 Connector

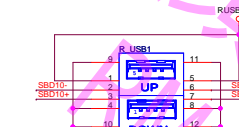




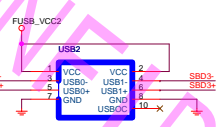
REAR USB PORT 6,7



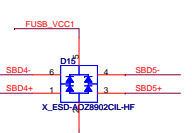
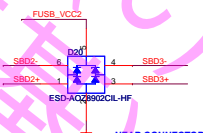
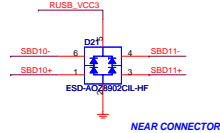
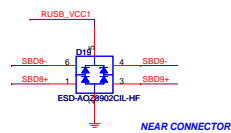
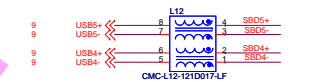
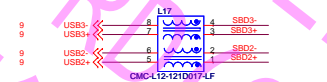
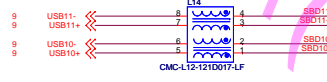
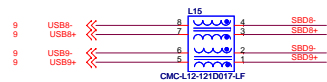
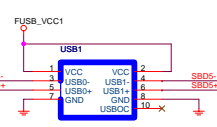
REAR USB PORT 10,11

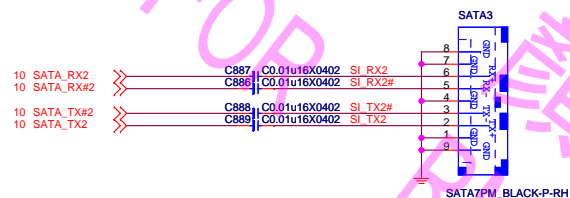
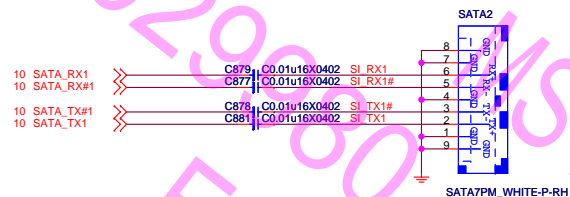
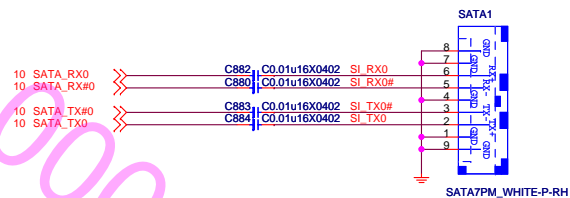


Front USB PORT 2,3

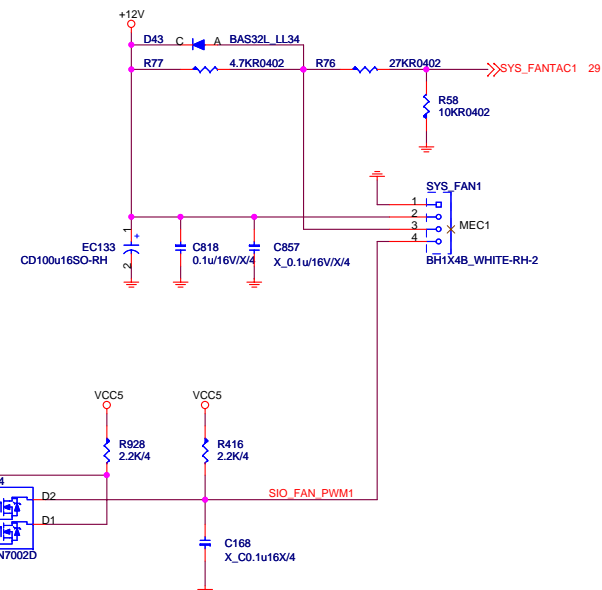


Front USB PORT 4,5

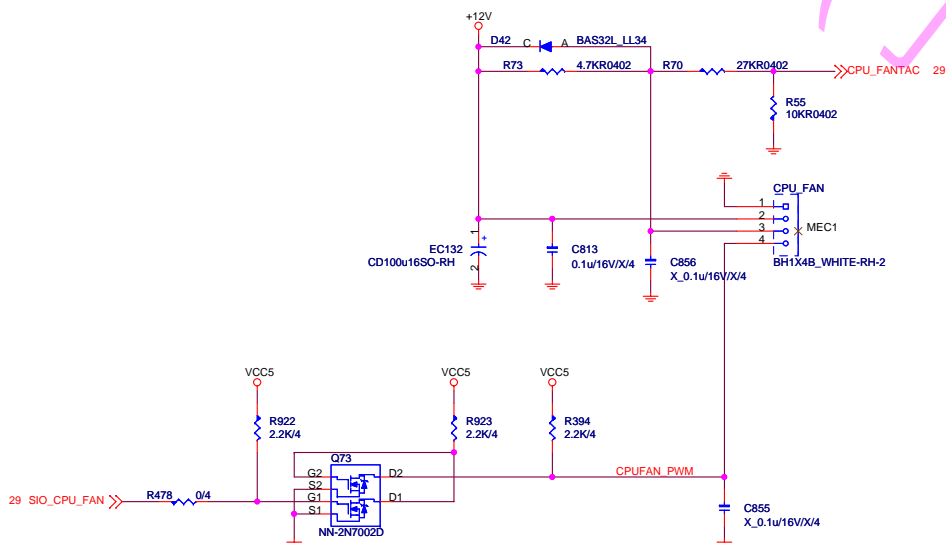




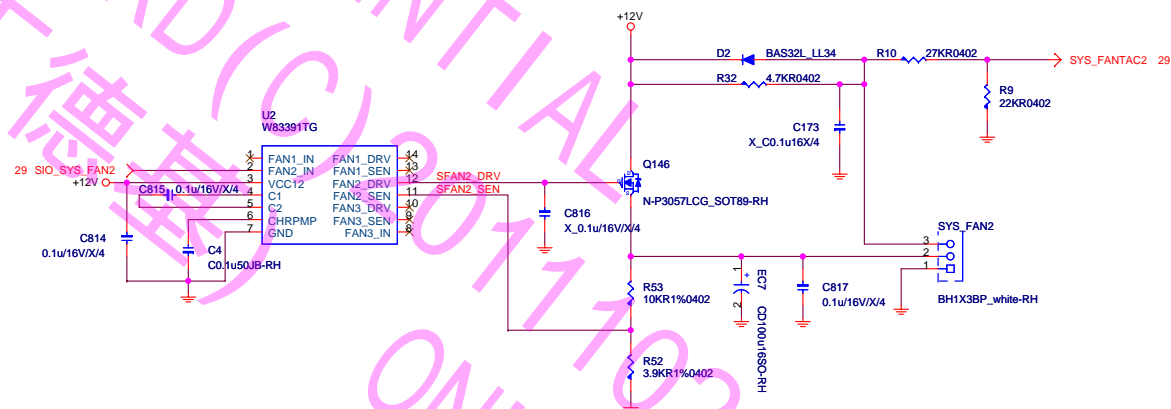
SYS Fan 1



CPU Fan



SYS Fan 2

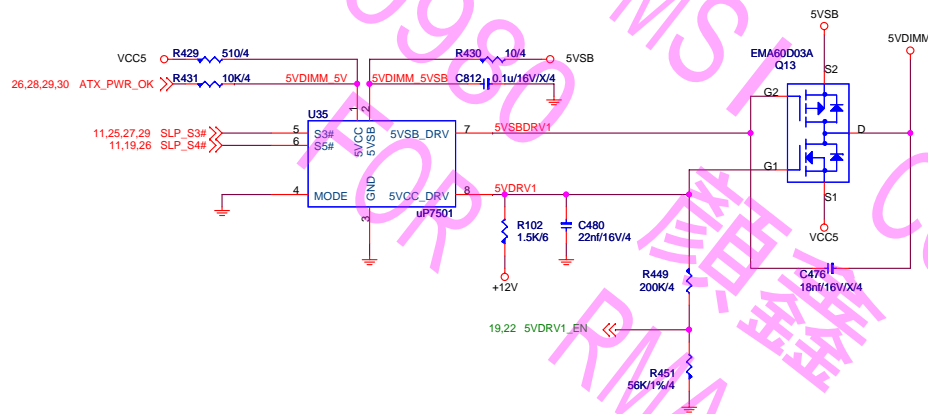


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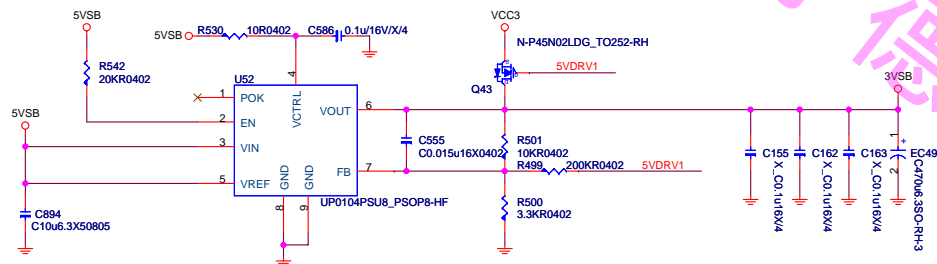
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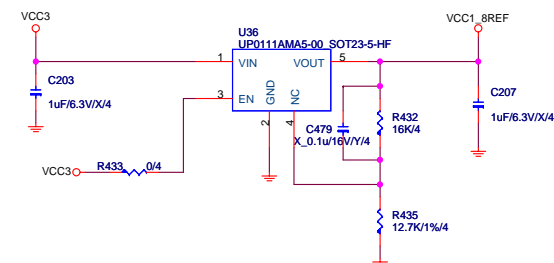
5VDIMM FOR DDR



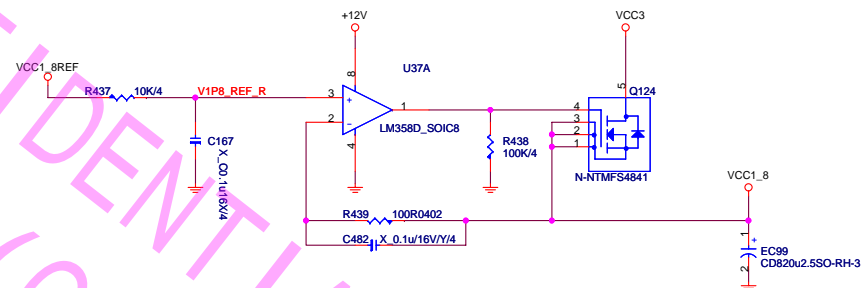
3VSB Power Rail



VCC1_8REF



CPU_PLL_1_8



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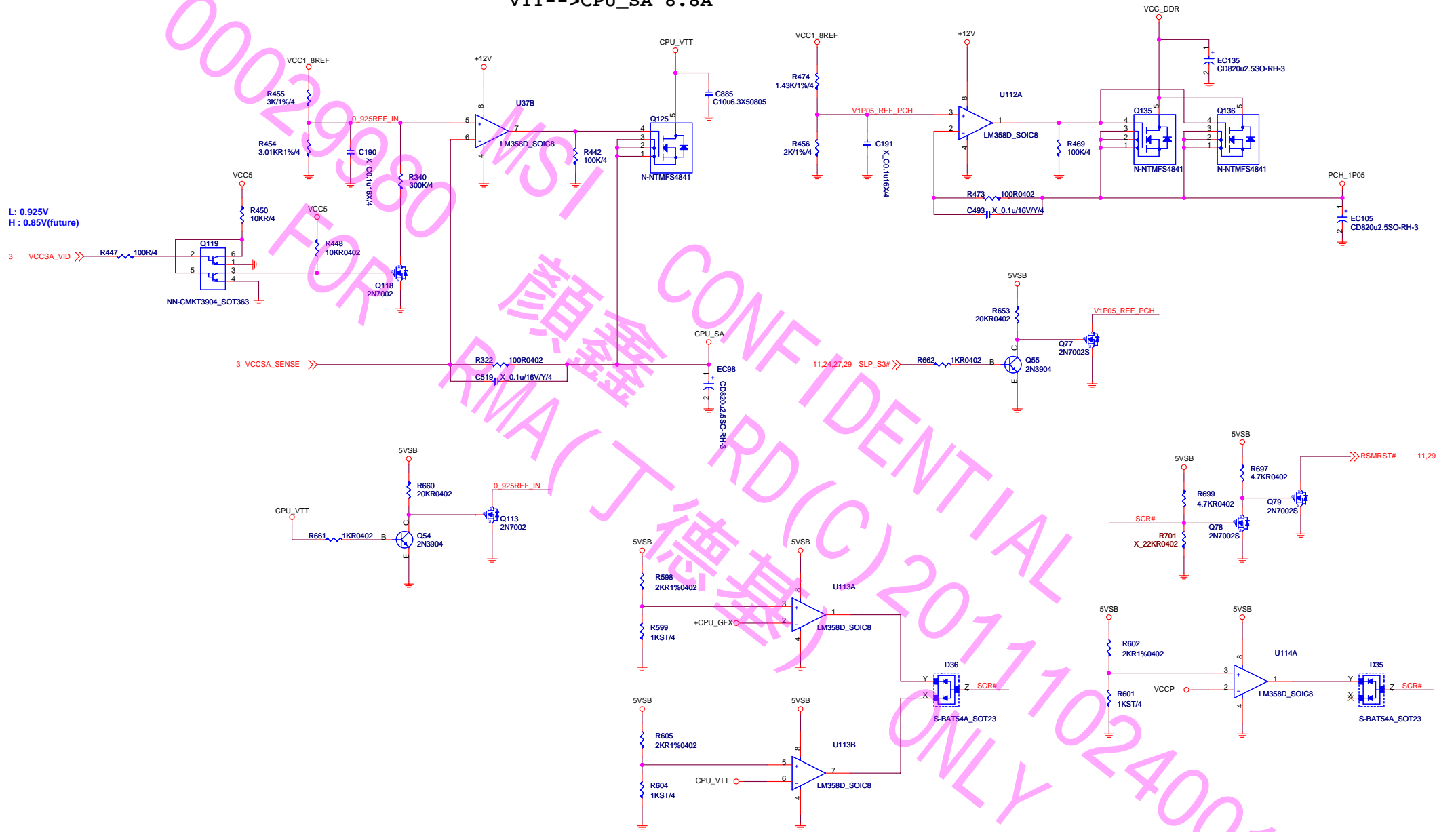
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Size: Custom Document Description: ACPI Controller UPI Rev: A00

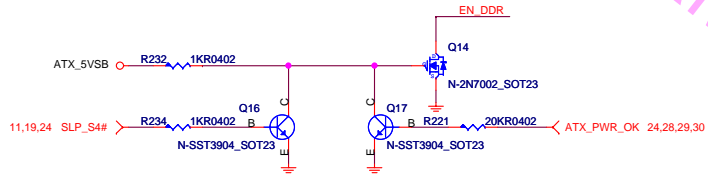
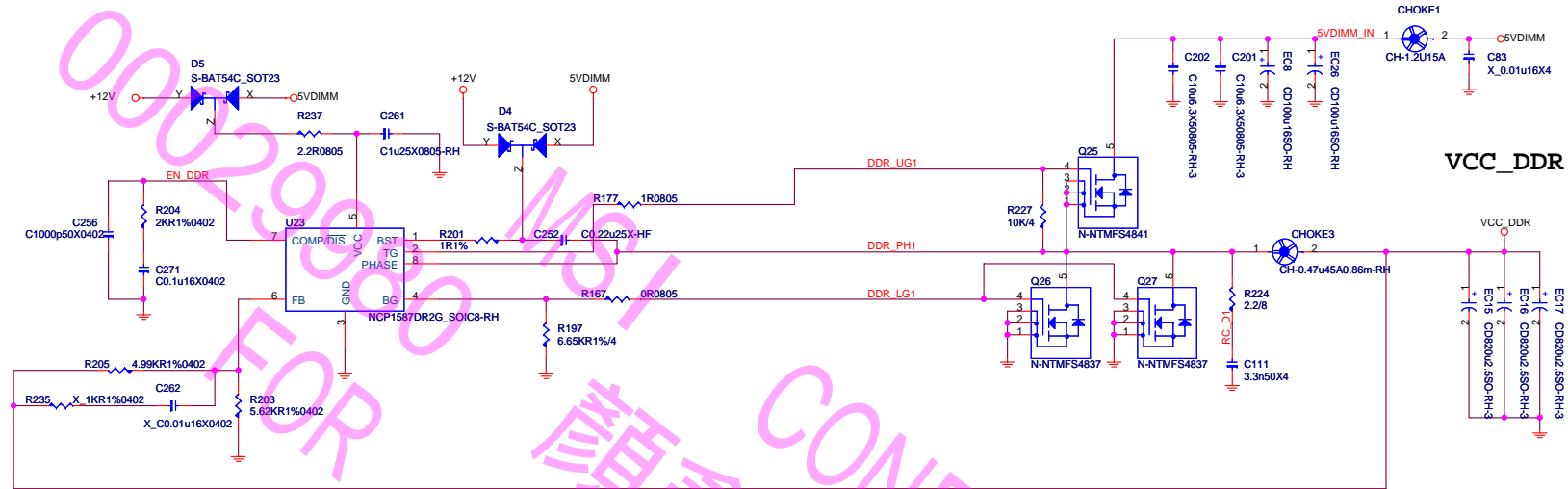
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VTT-->CPU_SA 8.8A

DDR-->PCH 6.2A

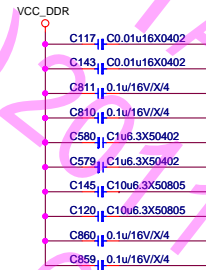
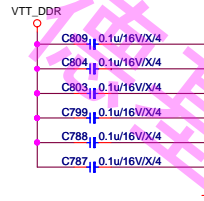
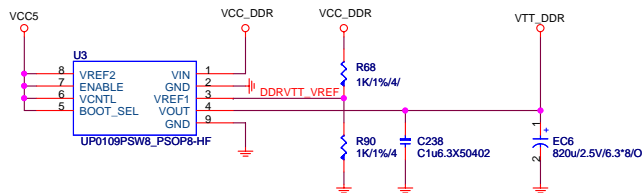


DDR III 1.5V POWER



DDR VTT Power

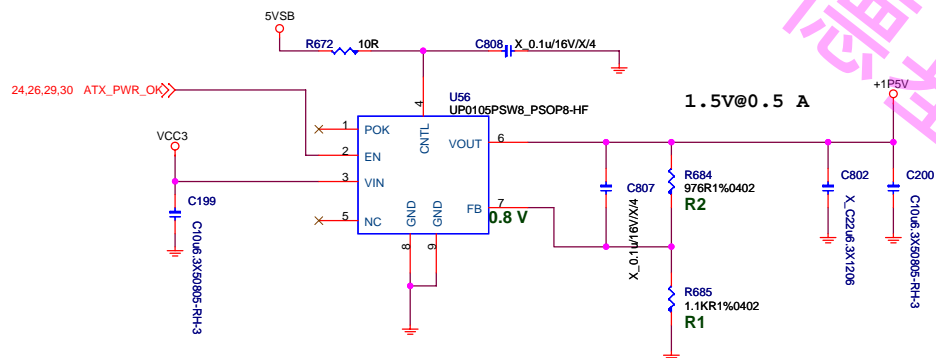
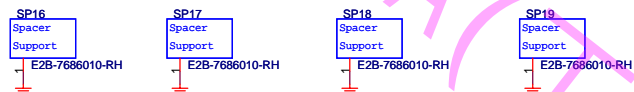
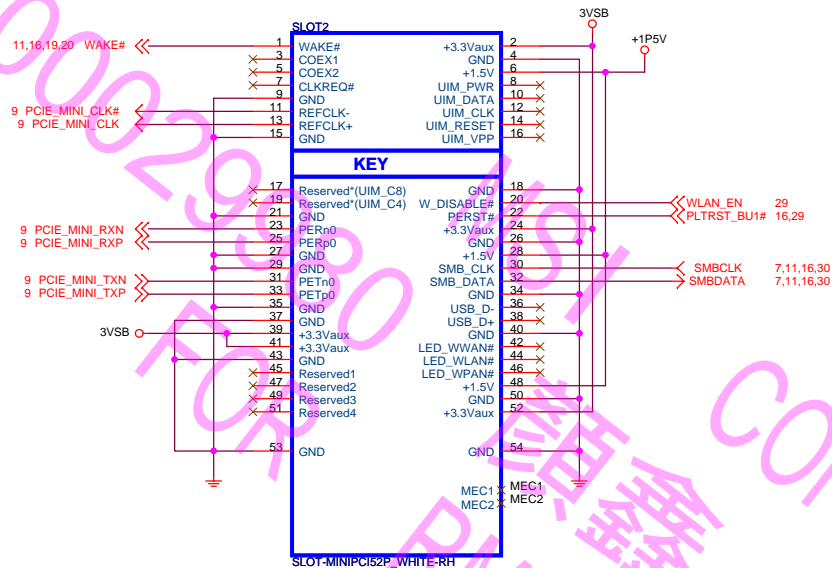
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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Size Custom

Document Description Mini slot

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ATX POWER CONNECTOR

PWR1

VCC3

-12V

3VSB

VCC5

VCC6

ATX_5VSB

+12V

VCC3

C771 0.1u/16V/X/4

C770 0.1u/16V/X/4

C769 0.1u/16V/X/4

R212 X_0R0805

C774 0.1u/16V/X/4

C805 0.1u/16V/X/4

C858 0.1u/16V/X/4

C776 0.1u/16V/X/4

3.3V

-12V

GND

P.ON

5V

5V

GND

-5V

5V

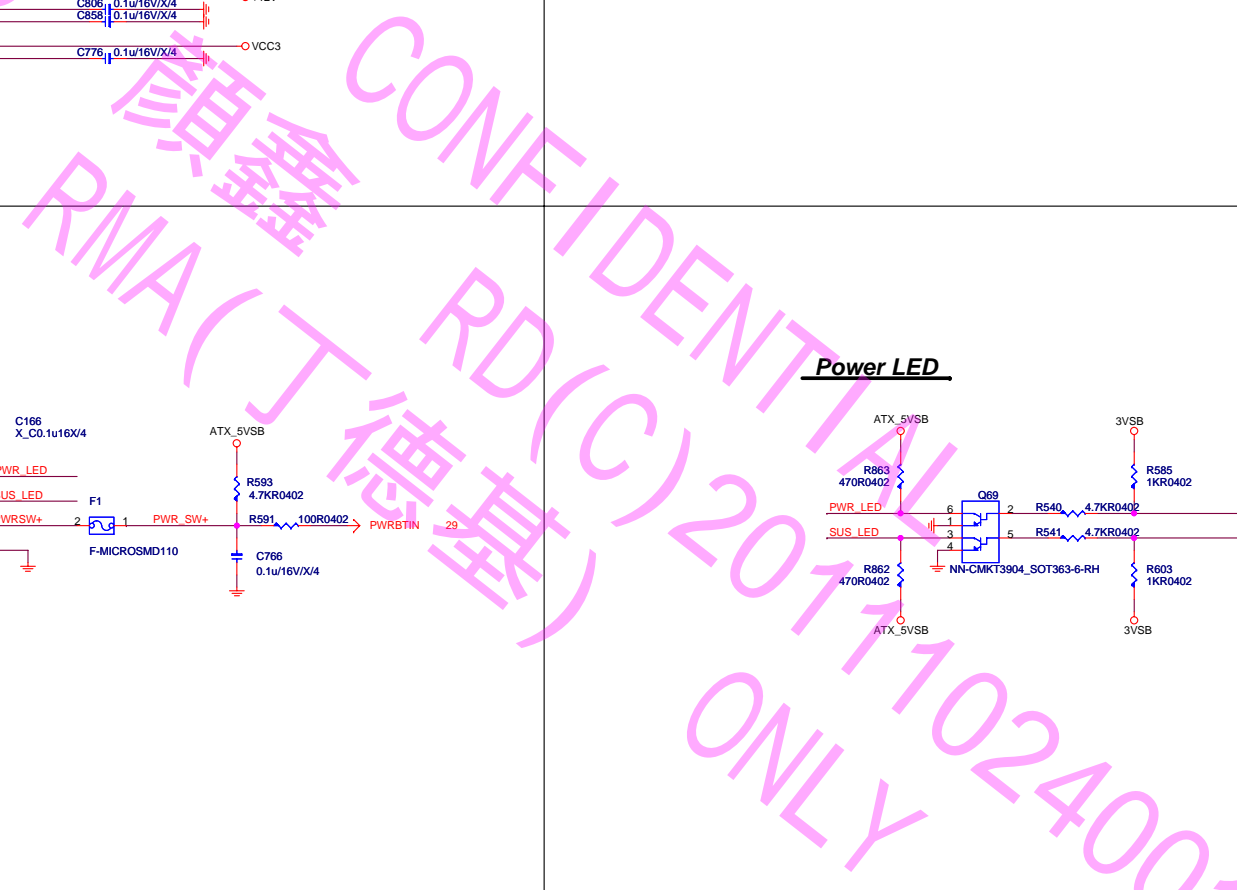
5VSB

5V

GND

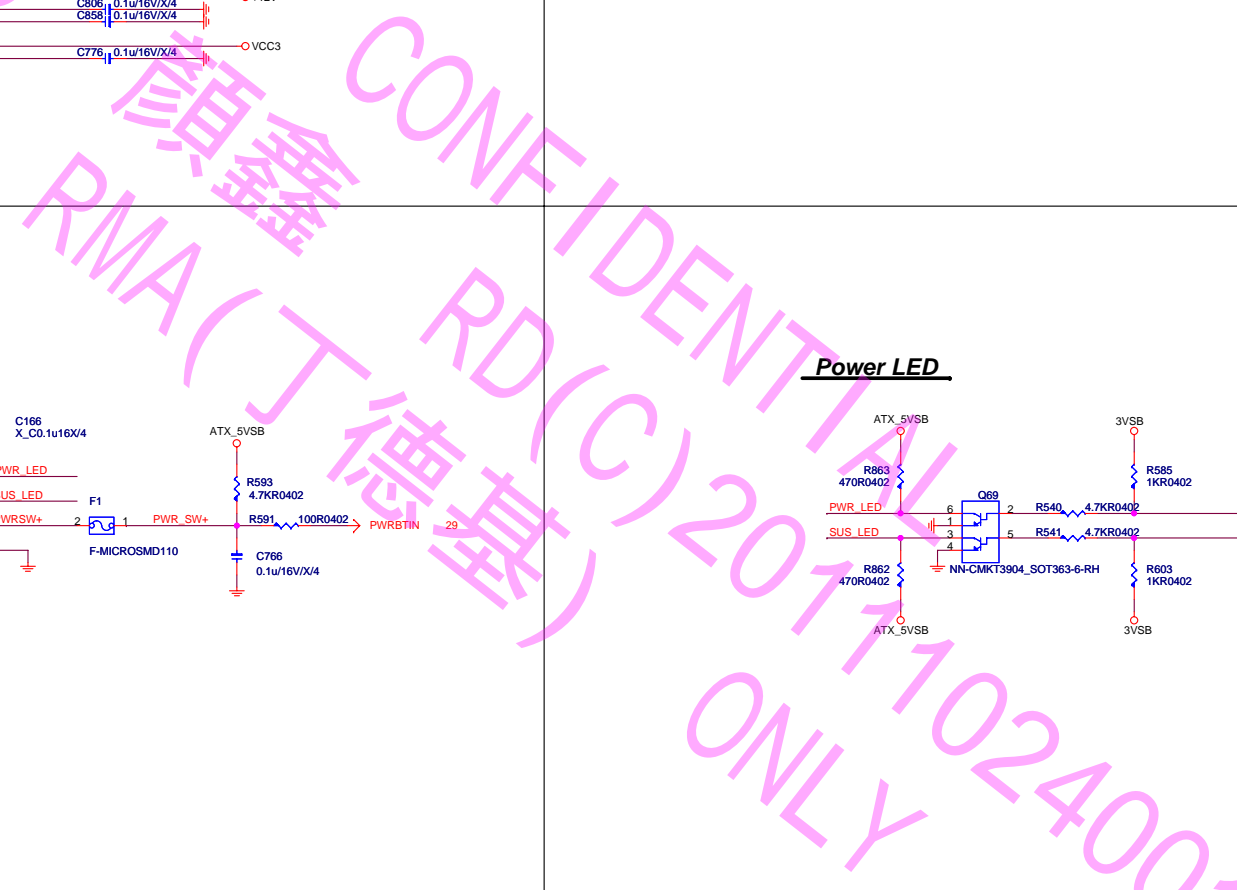
3.3V

PWRCONN24P_BLACK-RH-2



Buzzer Circuit

The diagram shows a buzzer circuit. A 5V supply (VCC5) is connected to the positive terminal of a buzzer (BZ1, BUZZER-LF). The negative terminal of the buzzer is connected to a diode (D44, BAS321_L1.34) in series with a 220 ohm resistor (R547, 220R0402). The other end of the resistor is connected to a common ground point. A capacitor (C777, 0.1u/16V/X4) is also connected to this common ground point. The diode's cathode is connected to a transistor (Q46, N-MMBT3904_NL_SOT23) in series with a 2.2K ohm resistor (R544, 2.2KR0402). The other end of the resistor is connected to a speaker (SPKR) and a red label '11,14'.



Front Panel

FRONT PANEL

H2X5[10]M_COLORS-RH

11 ODD_SW < R213 560R0402 1 HDD+ PLED 2 PWR_LED

11,16,28 SMBCLK > 3 HDD- SLED 4 SUS_LED

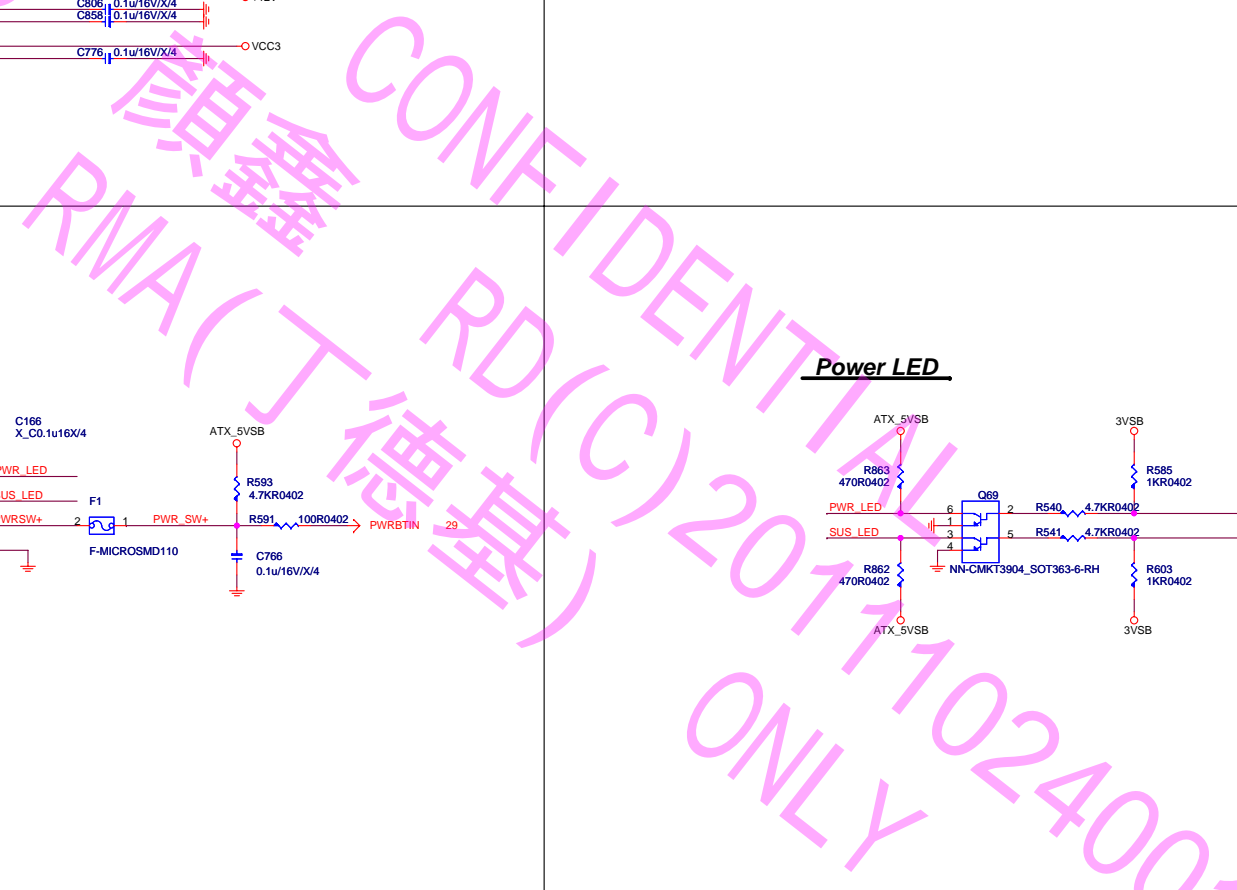
11,16,28 SMBDATA > 5 RESET- PWSW+ 6 PWRSW+ 2

7 RESET+ PWSW- 8

9 NC

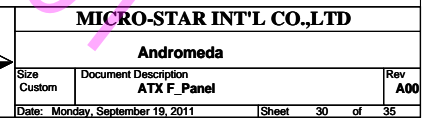
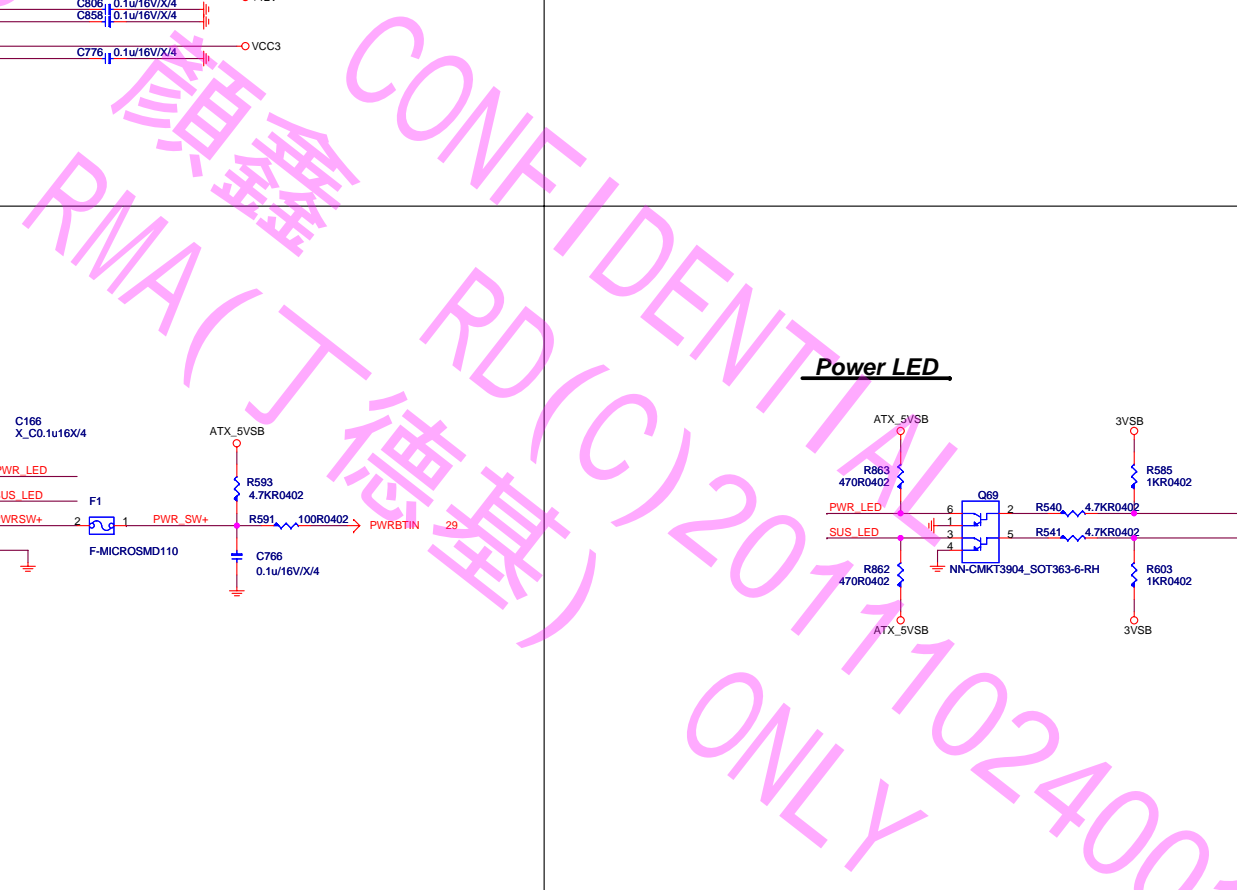
C166 X_C0.1u16X/4

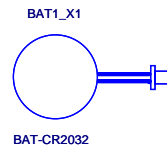
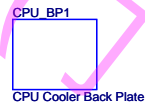
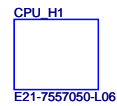
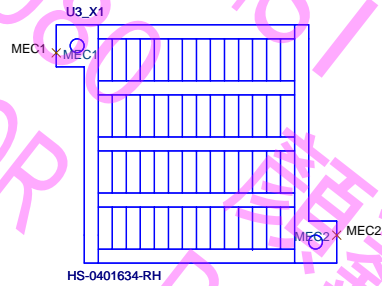
F1 F-MI



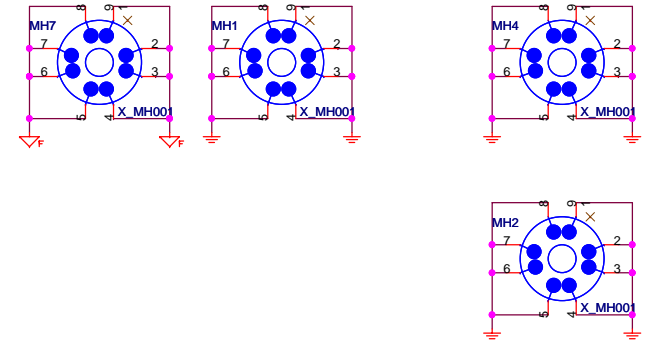
Power LED

The diagram illustrates the Power LED circuit. It features two LEDs, PWR_LED and SUS_LED, connected to an ATX 5VSB power source. The circuit includes resistors R863, R862, R540, R541, R585, and R603, all with a value of 470R0402. A MOSFET Q69 (NN-CMKT3904_SOT363-6-RH) is used to switch the LEDs. The LEDs are connected to a 3VSB source through resistors R585 and R603. The output of the LEDs is connected to LED_VCC and LED_VSB pins, which are labeled 29.

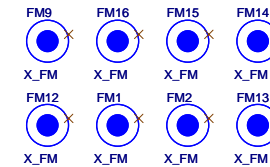




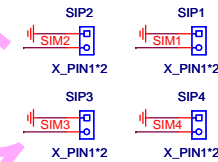
Mounting Holes



Optical Fiducial Marks-120



Simulation




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